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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,545	02/27/2004	Javier Arguelles	1406/186	7090

25297 7590 09/17/2007

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EXAMINER	
DEB, ANJAN K	

ART UNIT	PAPER NUMBER
2858	

MAIL DATE	DELIVERY MODE
09/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/788,545	ARGUELLES ET AL.	
	Examiner	Art Unit	
	Anjan K. Deb	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,13 and 14* is/are rejected.

7)☒ Claim(s) *5-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show in Figure 6 transistors T1-T6 as described in the specification (see abstract). Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "4" has been used to designate both "CORE" and "PAD" (see Fig. 6). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office

action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

The abstract of the disclosure is objected to because transistors T1-T6 are not shown in Fig. 6. Correction is required. See MPEP § 608.01(b).

The specification is objected to because references to claim numbers (claim 1)(see page 6 line 17 for example) should not appear in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 13, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oliva (US 2007/0188187) in view of Whetsel (US 6,731,106 B2).

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Re claim 1, Oliva disclosed switching circuit for a high speed data interface of an integrated circuit comprising switching transistors (504,802)(Fig. 5,8) for switching termination resistor 506 (Fig. 5) output stage (programmable resistance element), a data transmission signal path to a termination resistor 514 input stage (chip boundary) of a data reception signal path to form an internal feedback test loop (502, 506, pad, 508 forms the feedback loop shown in Fig. 5) within said integrated circuit.

Oliva did not expressly disclose switching transistors, which switch in a test mode.

Whetsel disclosed switching circuit for test mode operation for measuring on-resistance of an output stage (output buffer)(column 15 line 49).

At the time the invention was made it would have been obvious for one of ordinary skill in the art to modify Oliva et al. by including test mode operation disclosed by Whetsel in the impedance control circuit of Oliva for measuring on-resistance of output stage.

Re claims 2,3 Oliva disclosed switching circuit is connected to a configuration register 502 the termination resistor output stage 506 is programmable. The impedance element control circuit 502 is broadly interpreted as comprising configuration register since it produces one or more program control output signals to program or affect the programming of the programmable resistance element 506 (paragraph 0040).

Re claims 13 and 14, Oliva disclosed high speed data interface within an integrated circuit comprising: (a) a transmitting signal path for transmitting data via a data transmission line (output path from 506 to pad) which is connected to a termination resistor output stage 506 of said data transmission signal path, wherein the termination resistor output stage 506 is provided for adapting the output impedance of said data transmission signal path to a load (see claim 2 line 4) connected to said transmission data line; (b) a reception data signal path for receiving data via a data reception line (input line connected to pad), which is connected to a termination resistor 514 input stage of said data reception signal path, wherein the termination resistor 514 input stage is provided for adapting the input impedance of said data reception signal path to a load (claim 2 line 4) connected to said reception data line; and (c) a controllable switching circuit 502,504,506 comprising switching transistors for connecting termination resistor output stage 506 to the termination resistor input stage 514 to form an internal feedback test loop within said integrated circuit (502, 506, pad, 508 forms the feedback loop shown in Fig. 5).

Oliva did not expressly disclose controllable test switching circuit switching in a test mode.

Whetsel disclosed switching circuit for test mode operation for measuring on-resistance of an output stage (output buffer) (column 15 line 49).

At the time the invention was made it would have been obvious for one of ordinary skill in the art to modify Oliva et al. by including test mode operation disclosed by Whetsel in the impedance control circuit of Oliva for measuring on-resistance of output stage.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oliva (US 2007/0188187 and Whetsel (US 6,731,106 B2) in view of Wong (US 7,245,144 B1).

Re claim 4, Oliva disclosed switching circuit wherein the termination resistor output stage (506) is programmable (Fig. 5).

Oliva as modified by Whetsel did not expressly disclose termination resistor input stage is programmable but would have been obvious for input stage impedance matching.

Wong (US 7,245,144 B1) disclosed adjustable differential input and output drivers comprising adjustable termination resistances in input and output stage (drivers) to match the impedance on the differential signal lines (column 12 lines 18-27).

At the time the invention was made it would have been obvious for one of ordinary skill in the art to modify the combination system Oliva et al. and Whetsel by including programmable termination resistor in input stage for input stage impedance matching since Wong disclosed adjustable termination resistances in input stage to match the impedance on the differential signal lines.

Allowable Subject Matter

6. Claims 5-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claim 5 is allowable because the prior art does not teach or fairly disclose controllable test switching circuit comprises: a first transistor connected to said termination resistor output stage of the data transmission signal path a second transistor connected between said first transistor and a reference potential node; a third transistor connected between said reference potential node and a sixth transistor; a fourth transistor connected between said first transistor and a test node; a fifth transistor connected between said test node and said sixth transistor; wherein the sixth transistor is connected to said termination resistor input stage of the data reception signal path.

Claims 6-12 depend from claim 5 and are also allowable for the same reasons as above.

Conclusion

7 . The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Baird (US 2007/0057736) disclosed feedback system incorporating switching termination resistor 412, 439 (fig. 20).

Wong (US 6,864,704 B1) disclosed switching circuits (Fig. 6) for selecting termination resistors (Fig. 11a.11b) for adjustable differential input and output drivers.

Wong (US 6,879,131 B2) disclosed programmable resistors for integrated circuits.

Yang (US 6,590,413 B1) disclosed switching control circuit 104 for self-tracking integrated differential termination resistance R_{TERM} (Fig. 1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Anjan K. Deb whose telephone number is 571-272-2228. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew H. Hirshfeld can be reached at (571) 272-2168.

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